IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Technology Center 2600

Applicants

: John D. Porter and William N. Thompson

Serial No. Filed

: 09/750,174

: December 18, 2000

Title

: LATCH-UP PREVENTION FOR MEMORY CELLS

Docket No

: MIO\0042 V2

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington,

ember 5, 2001

Assistant Commissioner for Patents

Washington, D.C. 20231

Wronglicat

Thomas E. Lees

Sir:

THIRD PRELIMINARY AMENDMENT

IN THE DRAWINGS

Being filed concurrently here with is a separate paper entitled "Proposed Drawing Corrections." Enclosed with that paper is a redline copy of Fig. 4A indicating the proposed changes. It is submitted that these changes to the drawings do not introduce new matter into the application. Approval of the proposed changes is hereby requested.

REMARKS

Figure 4A is a schematic representation of the invention as shown in Figure 4B. Figure 4A should be changed to show that the emitter of parasitic transistor 74 is coupled to the input voltage Vcc through the resistance 44 as shown in Figure 4B and described in the specification at page 19, lines 1-6. The change does not constitute new matter and is made only to ensure that Figure 4A accurately depicts the claimed invention. Approval of the proposed changes is hereby respectfully requested.

Applicants respectfully submit that the present application is in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters Serial No. 09/750,174 Docket No. MIO 0042 V2

or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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